19-1419; Rev 5; 4/00

MAXIM

MAX3675/MAX3676 Evaluation Kits

Evaluate: MAX3675/MAX3676

General Description

The MAX3675/MAX3676 evaluation kits (EV kits) simplify evaluation of the MAX3675/MAX3676 622Mbps clock-recovery and data-retiming IC with limiting amplifier. The EV kits enable testing of all MAX3675/MAX3676 functions. They provide selectable analog or digital data inputs, as well as differential PECL-compatible data and clock outputs.

The differential data and clock outputs have 50Ω attenuators on-board to allow direct connection to a high-speed oscilloscope.

The MAX3675/MAX3676 EV kits come configured for +3.3V operation and consume approximately 120mA.

Component Suppliers

SUPPLIER	PHONE	FAX
Coilcraft	847-639-6400	847-639-1469

Features

- **SMA Connections for all Data and Clock I/Os**
- **Test Points for Monitoring**
  - **Received-Signal-Strength Indicator (RSSI)**
  - **Loss-of-Power (LOP)**
  - **Loss-of-Lock (LOL)**
  - **LOP Threshold Level (V_{TH})**
- **+3.3V Single-Supply Operation**
- **Fully Assembled and Tested**

Ordering Information

PART	TEMP. RANGE	IC PACKAGE
MAX3675EHJEVKIT	-40°C to +85°C	5mm 32 TQFP
MAX3676EHJEVKIT	-40°C to +85°C	5mm 32 TQFP

Component List

DESIGNATION	QTY	DESCRIPTION
C1–C4, C7–C10, C13, C21, C23, C25, C27	13	0.1µF, 25V ceramic capacitors
C5, C6, C14	3	0.01µF, 25V ceramic capacitors
C12	1	2.2µF ±20% X7R ceramic cap or 16V (min) tantalum capacitor
C22, C24, C26, C28, C29, C30	6	100pF, 25V ceramic capacitors
C20	1	2.2µF, 25V ceramic capacitor
C11, C16	0	Open
C15	1	0.047µF, 25V ceramic capacitor
C17	1	0.033µF, 25V ceramic capacitor
C19	1	33µF ±20% capacitor
L1, L2	0	Not included. Use a 56nH inductor for additional power-supply decoupling, if needed.
L3, L4	2	56nH inductors Coilcraft 0805HS-560TKBC
R2, R4, R9, R13, R17, R21	6	130Ω ±1% resistors
R1, R3	2	82.5Ω ±1% resistors
R5, R6	2	49.9Ω ±1% resistors
R7, R11, R15, R19	4	24.3Ω ±1% resistors
R8, R12, R16, R20	4	27.4Ω ±1% resistors

DESIGNATION	QTY	DESCRIPTION
R10, R14, R18, R22	4	221Ω ±1% resistors
R23	1	52.3Ω ±1% resistor (MAX3675EHJ)
R23	1	0Ω resistor (MAX3676EHJ)
R24	1	3kΩ ±5% resistor
R25	1	3.3kΩ ±5% resistor
R26	1	10kΩ potentiometer
R27	1	20kΩ ±5% resistor
R28, R32, R33	3	10kΩ ±5% resistors
R29	1	120kΩ ±5% resistor
R31	1	100kΩ potentiometer
R30	1	0Ω resistor
DDI+, DDI-, ADI+, ADI-, SDO+, SDO-, SCLKO+, SCLKO-	8	SMA connectors
V_{CC}, JP1, JP2, GND	4	2-pin headers
JP4, JP5, JP6, JP7, JP9	5	Not Installed
JP8, JP10	2	3-pin headers
TP1–TP4	6	1-pin headers
None	3	Shunts for JP2, JP8, and JP10
U1	1	MAX3675EHJ or MAX3676EHJ
None	1	MAX3675 or MAX3676 data sheet

Detailed Description

The MAX3675/MAX3676 EV kits are fully assembled and factory tested. They enable testing of all MAX3675/MAX3676 functions.

Test Equipment Required

- +3.3V power supply with 200mA current capability
- Signal-source, 622Mbps BER test set
- Jitter analyzer capable of 622Mbps performance
- Oscilloscope with at least 1GHz performance

Connections

The digital inputs (DDI+, DDI-) have on-board AC-coupling capacitors followed by Thevenin-equivalent 50Ω terminations. The analog inputs (ADI+, ADI-) are equipped with DC 50Ω loads followed by AC-coupling capacitors. Remember that the analog inputs to the MAX3675/MAX3676 must be AC-coupled. All of the MAX3675/MAX3676 data and clock outputs (SDO+, SDO-, SCLKO+, SCLKO-) are terminated on-board with 50Ω, PECL, 2X attenuators. Configured in this way, these outputs can be directly connected to the 50Ω inputs of a high-speed oscilloscope for analysis.

Setup

1) Select either the PECL (DDI ENABLE) or the analog (ADI ENABLE) inputs with jumper JP10.
2) Verify that the shunt across jumper JP2 is in place.
3) Verify that the shunt is across pins 2 and 3 of jumper JP8.
4) Verify that resistor R23 is 52.3Ω (MAX3675) or 0Ω (MAX3676).
5) Connect the +3.3V power supply to the appropriate terminals marked on the EV kit and apply power.
6) Connect a 622Mbps PRBS NRZ signal to the selected inputs with 50Ω cables.
7) Connect the outputs to a 50Ω high-speed oscilloscope.

Jitter analysis and product performance can also be observed by appropriately interfacing the EV kit with a bit-error-rate tester (BERT) and a jitter analyzer.

Interfacing with ECL Test Equipment

Not all jitter analyzers and BERTs can easily interface with the EV kits' PECL output signal levels. If your test equipment requires standard ECL levels, then bias tees are required (Figure 1). For example, if using an HP BERT, you must do the following:

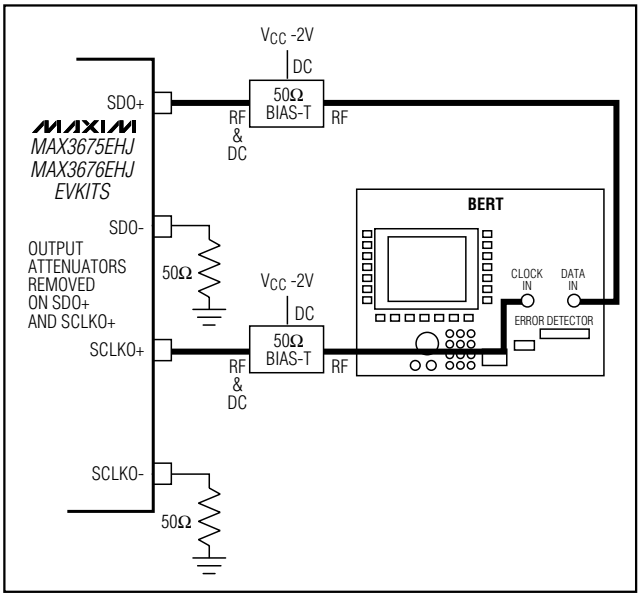

Figure 1. ECL Interface to Test Equipment

1) Remove the data and clock output attenuators for those signal lines you intend to observe. For example, if you intend to observe SDO+, then open R9 and R10, and short R7 and R8.
2) Use a 50Ω bias tee to bias the MAX3675/MAX3676 outputs.

Adjustments, Jumpers, and Test Points

Two adjustments are available on the MAX3675/ MAX3676 EV kits: VTH ADJ (R31) and PHADJ (R26). VTH ADJ is used to set the loss-of-power threshold level for the LOP monitor. PHADJ, although not required, can be used to shift the sampling edge of the recovered clock relative to the center of the data eye. Be sure to remove jumper JP2 if you intend to adjust PHADJ. See Table 1 for jumper functions.

The following high-impedance test points are provided for signal monitoring:

- RSSI, used to monitor the received-signal-strength indicator output
- LOP, used to monitor loss of power
- $\overline{LOL}$, used to monitor loss of lock
- V_{TH}, used to monitor the threshold voltage level

Table 1. Jumper Functions

NAME	TYPE	DESCRIPTION	NORMAL POSITION
JP1	2-Pin	Disables the MAX3675/ MAX3676 loop filter	Open (enabled)
JP2	2-Pin	Disables the phase adjustment (R26)	Shorted (disabled)
JP4, JP5, JP6, JP7	2-Pin	Not supplied. The PC board trace between jumper pads can be cut open if analysis requires	Shorted
JP8	3-Pin	Disables VTH adjustment (R31)	Pins 2 and 3 shorted (enabled)
JP10	3-Pin	Used to select between the digital inputs (DDI ENABLE) and the analog inputs (ADI ENABLE) of the MAX3675/MAX3676	—

Layout Considerations

MAX3675/MAX3676 performance can be greatly affected by circuit board layout and design. Use good high-frequency design techniques, including minimizing ground inductances and using fixed-impedance transmission lines on the data and clock signals.

MAX3675/MAX3676 Evaluation Kits

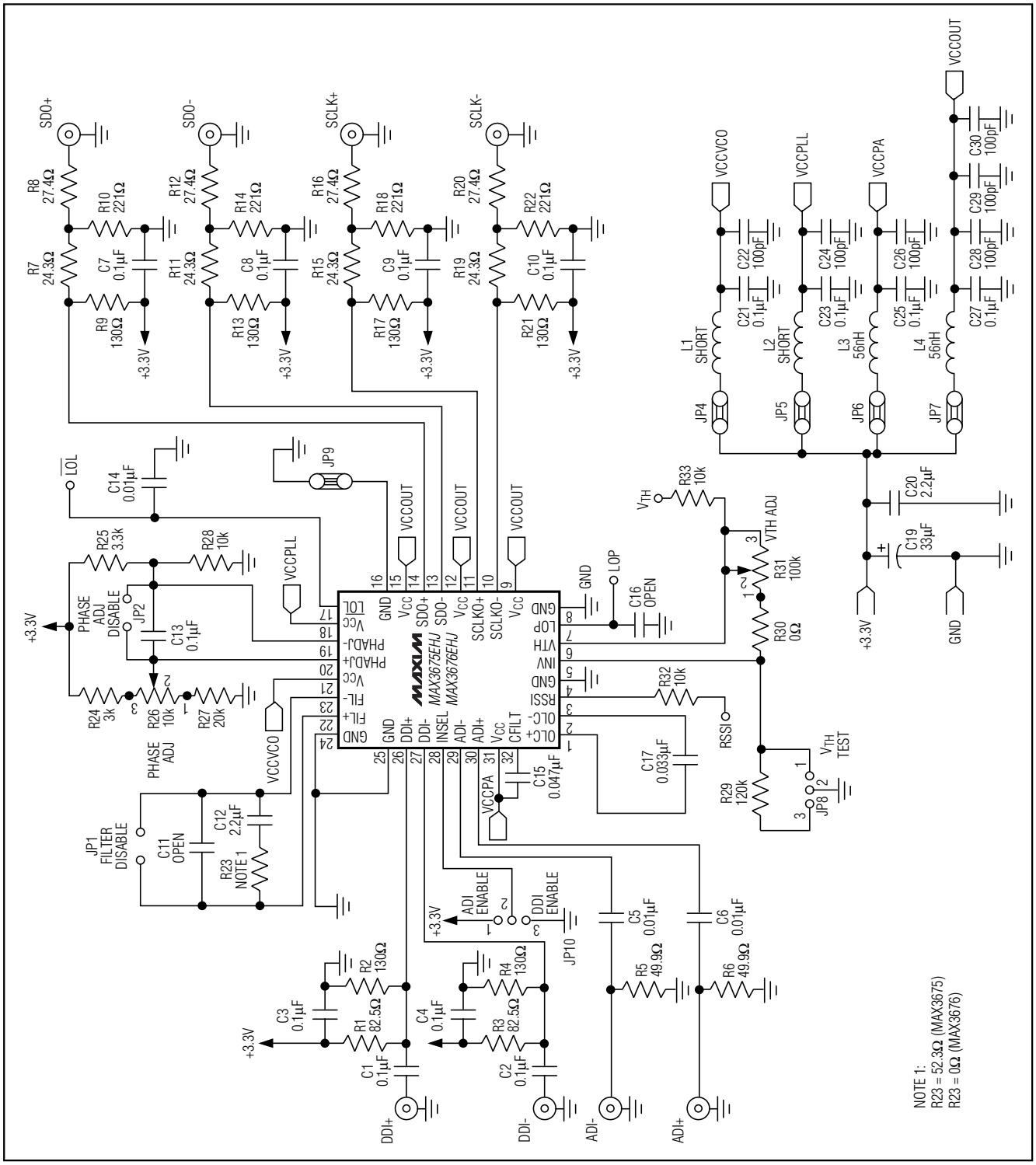

Figure 2. MAX3675/MAX3676EHJ EV Kits Schematic

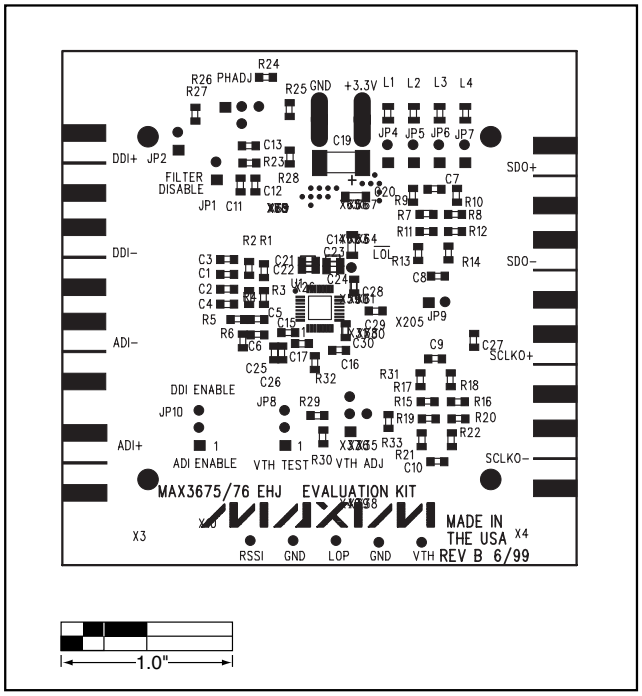

Figure 3. MAX3675/MAX3676 EV Kits Component Placement Guide

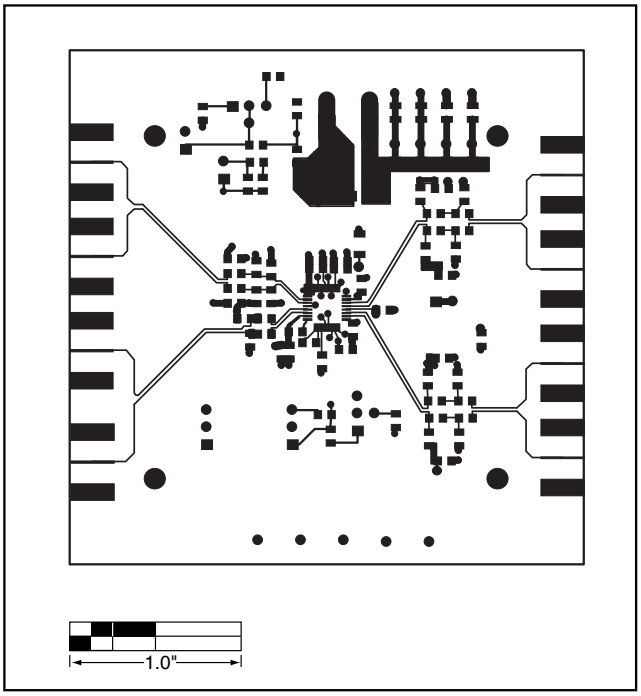

Figure 4. MAX3675/MAX3676 EV Kits PC Board Layout—Component Side

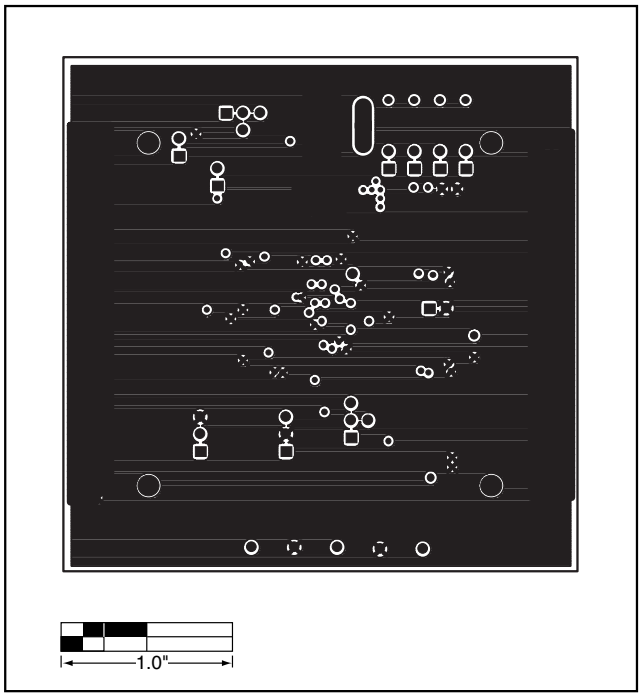

Figure 5. MAX3675/MAX3676 EV Kits PC Board Layout—Ground Plane

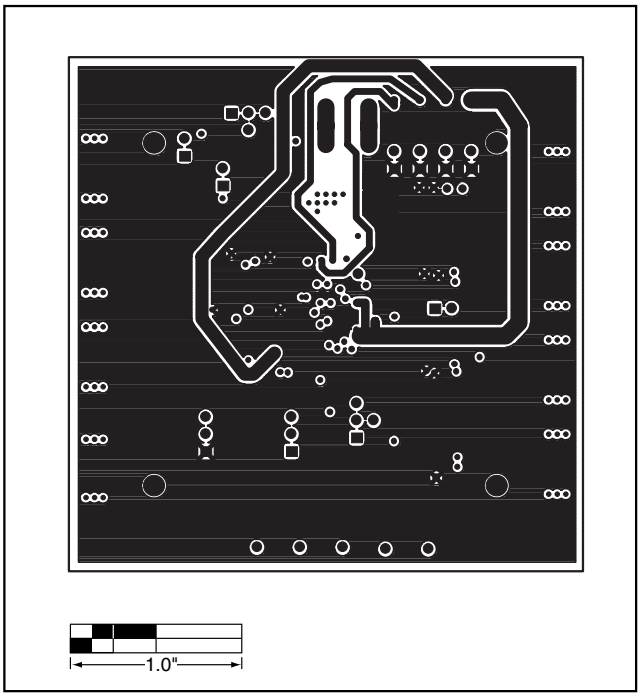

Figure 6. MAX3675/MAX3676 EV Kits PC Board Layout—Power Plane

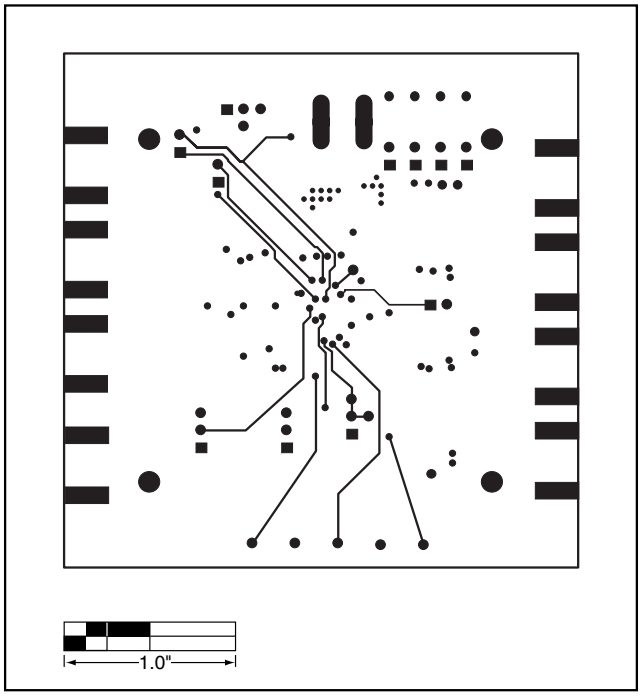

Figure 7. MAX3675/MAX3676 EV Kits PC Board Layout—Solder Side